

#2/59-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Toshitake YAEGASHI

SERIAL NO: New Application

GAU:

FILED: Herewith

EXAMINER:

FOR: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.



REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION


- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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**STATEMENT OF RELEVANCY**

**Reference AO (11-224909) of Form PTO-1449.**

This reference shows a similar sectional view of memory cell and select-gate transistor. (Fig. 4 and lines 33 - 44 of right portion of page 13 and lines 10 - 14 of left portion of page 14).

**Reference AP (10-209405) of Form PTO-1449.**

This reference shows a similar sectional view of memory cell and select-gate transistor. (Fig. 3 and lines 29 - 38 of right portion of page 8).

**Reference AQ (2000-68487) of Form PTO-1449.**

This reference shows a similar sectional view of memory cell and select-gate transistor. (Fig. 2 and lines 4 - 26 of right portion of page 3).